

Serial No. 09/874,032

1. (Presently amended) A charge detection device for use in an image sensor, said charge detection device including a vertical punch-through transistor ~~having the gate surrounding the source and being conductively connected to the source~~ having a gate surrounding a source and being conductively connected to the source.

2. (Previously amended) The device according to claim 1, wherein a charge present under the gate modulates the punch through potential barrier of the vertical punch-through transistor.

3. (Previously amended) The device according to claim 2, including a charge reset means adjacent to and coupled to the vertical punch-through transistor to remove charge therefrom.

4. (Cancelled)

5. (Cancelled)

6. (Cancelled)

7. (Currently amended) A CMOS device comprising:
an image sensor; and
a charge detection device in said image sensor including a vertical punch-through transistor ~~having the gate surrounding the source and being conductively connected to the source.~~ having a gate surrounding a source and being conductively connected to the source.

8. (Previously amended) The device according to claim 7, wherein a charge present under the gate modulates the punch through potential barrier of the vertical punch-through transistor.

9. (Previously amended) The device according to claim 8, including a charge reset means adjacent to and coupled to the vertical punch-through transistor to remove charge therefrom.

10. (Previously amended) The device according to claim ~~8~~ 9, wherein the charge reset means is an MOS reset gate.

11. (Cancelled)

12. (Cancelled)

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13.(Previously Added) A CCD device comprising:
an image sensor; and
a charge detection device in said image sensor including a vertical punch-through transistor having the gate surrounding the source and being conductively connected to the source.

14.(Previously Added) The device according to claim 13, wherein a charge present under the gate modulates the punch through potential barrier of the vertical punch-through transistor.

15.(Previously Added) The device according to claim 14, including a charge reset means adjacent to and coupled to the vertical punch-through transistor to remove charge therefrom.

16.(Previously Added) The device according to claim 15, wherein the charge reset means is an MOS reset gate.